USN | | | | | | | | | | |

06ELN15/25

First/Second Semester B.E. Degree Examination, December 2011
Basic Electronics

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions choosing at least TWO from each part.*
2. Answer all objective type questions only in OMR sheet page 5 of the Answer Booklet.
3. Answer to objective type questions on sheets other than OMR will not be valued.

PART – A

1 a. Select the correct answer :

i) The peak inverse voltage is the peak voltage across the diode when the diode is _____ biased.
A) forward B) Reverse C) Unbiased D) All of these.

ii) The reverse saturation current doubles at every _____ rise in temperature.
A) 20°C B) 40°C C) 10°C D) None of these.

iii) The ripple factor of full wave rectifier without filter is about
A) 40.6 B) 0.483 C) 1.21 D) 0.812

iv) The average dc voltage of a full wave rectifier is
A) V_m/π B) $V_m/2$ C) $2V_m/\pi$ D) V_m **(04 Marks)**

b. With a neat circuit diagram and relevant waveforms, explain the operation of a full wave bridge rectifier. **(07 Marks)**

c. A diode with a 700 mW maximum power dissipation at 25°C has a 5 mW/°C devating factor. If the forward voltage drop remains constant at 0.7V, calculate the maximum forward current at temperatures 25°C and 65°C. **(05 Marks)**

d. Define line regulation and load regulation. **(04 Marks)**

2 a. Select the correct answer :

i) The arrow in the graphic symbol of a transistor defines the direction of _____ current.
A) base B) collector C) emitter D) None of these.

ii) In the cutoff region, emitter-base junction is
A) forward biased B) reverse biased C) unbiased D) None of these.

iii) The common-base current gain (α_{dc}) of a transistor is given by
A) I_C / I_B B) I_C / I_E C) I_E / I_C D) None of these.

iv) In the common-emitter configuration, I_{CEO} is given by
A) I_{CBO} B) βI_{CBO} C) $(1 + \beta) I_{CBO}$ D) None of these. **(04 Marks)**

b. Sketch the typical transistor input and output characteristics for the CE configuration. Briefly explain the three regions of operation. **(07 Marks)**

c. Explain the procedure for drawing the DC load line on the transistor CE output characteristics. In the circuit shown in Fig.Q2(c), a silicon transistor with $\beta_{dc} = 100$ is used. Draw the DC load line on output characteristics and indicate Q-point. **(09 Marks)**

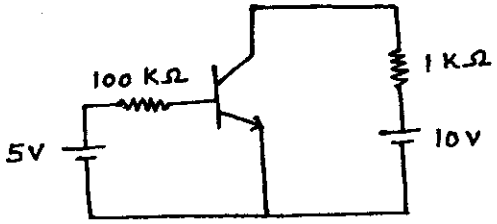

Fig.Q2(c)

3 a. Select the correct answer :

i) The Q-point will shift if _____ changes.

A) temperature B) β_{dc} C) I_{CBO} D) All the these.

ii) For the base-bias circuit, if the base current is 30 μA and β_{dc} is 100, then the value of I_C is

A) 3 mA B) 30 mA C) 3 μA D) 100 mA.

iii) The stability factor S for the base bias circuit is

A) β B) 1/β C) 1 + β D) None of these.

iv) The value of R_T in voltage divider bias circuit is

A) $R_1 + R_2$ B) $\frac{R_1R_2}{R_1+R_2}$ C) R_1R_2 D) None of these. **(04 Marks)**

b. Sketch the circuit of voltage divider bias and discuss its approximate analysis. **(08 Marks)**

c. Calculate the maximum and minimum levels of I_C and V_{CE} for the bias circuit shown in Fig.Q3(c), when $h_{FE(min)} = 50$ and $h_{FE(max)} = 200$. Assume $V_{BE} = 0.7$. **(08 Marks)**

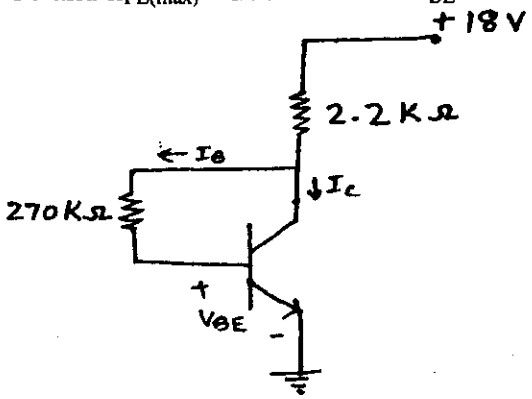

Fig.Q3(c)

4 a. Select the correct answer :

i) SCR is a _____ device.

A) bidirectional B) unidirectional

C) both unidirectional and bidirectional D) None of these.

ii) _____ is the minimum current that should flow through a SCR to maintain it in the ON state.

A) Maximum RMS current B) Gate trigger current

C) Holding current D) None of these.

a. iii) UJT is a three terminal device with a _____ pn-junction.
A) double B) single C) three D) None of these.

iv) FET is a _____ controlled device.
A) Current B) power C) voltage D) None of these. **(04 Marks)**

b. Draw the circuit diagram to show how an SCR can be triggered by application of a pulse to the gate terminal. Sketch the circuit waveforms and explain it operation. **(08 Marks)**

c. Draw and explain the family of drain characteristics for a n-channel JFET. **(08 Marks)**

PART – B

5 a. Select the correct answer :

i) Two amplifiers with voltage gains 10 and 100, are connected in cascade. The overall voltage gain is
A) 100 B) 90 C) 1000 D) 10

ii) To obtain the sustained oscillations in a sinusoidal oscillator, the loop gain should be equal to
A) 1 B) ∞ C) 0 D) None of these.

iii) For a RC phase shift oscillator, the frequency of oscillations is given by
A) $1 / 2\pi RC$ B) $1 / 2\pi RC\sqrt{6}$ C) $1 / 2\pi RC\sqrt{3}$ D) None of these.

iv) An oscillator uses _____ type of feedback.
A) negative B) positive C) zero D) None of these. **(04 Marks)**

b. Draw and explain the circuit of a two stage RC coupled common-emitter amplifier. Explain the frequency response of this amplifier. **(08 Marks)**

c. Draw the circuit of a transistor Colpitt's oscillator and explain its operation. Calculate the frequency of oscillations with $C_1 = C_2 = 400$ PF and L = 2 mH. **(08 Marks)**

6 a. Select the correct answer :

i) An ideal op-amp has _____ slew rate.
A) 0 B) ∞ C) unity D) None of these.

ii) The supply voltage or power supply rejection ratio of an ideal op-amp is
A) ∞ B) 0 C) 1 D) None of these.

iii) An op-amp can be used as
A) adder B) integrator C) voltage follower D) All of these.

iv) In an inverting amplifier, there is _____ phase shift with input and output.
A) 90° B) 180° C) 0° D) 360° **(04 Marks)**

b. Explain how an op-amp can be used as a differentiator. **(04 Marks)**

c. For the circuit shown in Fig.Q6(c), calculate the output voltage. V_o. **(06 Marks)**

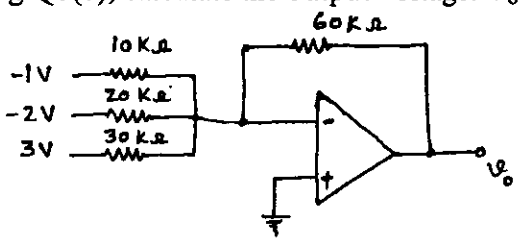

Fig.Q6(c)

d. Explain how the amplitude, frequency and time period are measured using a CRO. **(06 Marks)**

7 a. Select the correct answer :

i) $(76.6)_8 = (\ ?\ )_2$

A) $(111110.110)_2$ B) $(110110.110)_2$ C) $(111100.110)_2$ D) $(101100.100)_2$

ii) $(15)_{10} = (\ ?\ )_{BCD}$

A) $(11010110)_{BCD}$ B) $(00010101)_{BCD}$ C) $(10010101)_{BCD}$ D) $(00100101)_{BCD}$

iii) 2's complement of binary number 10101 is

A) 00011 B) 01010 C) 01011 D) 10010

iv) $(39)_{10} = (\ ?\ )_2$

A) $(100111)_2$ B) $(100110)_2$ C) $(110101)_2$ D) $(111001)_2$ **(04 Marks)**

b. Explain the principle of amplitude modulation with the suitable waveforms. Derive the expression for AM wave. **(08 Marks)**

c. Compare AM and FM. **(04 Marks)**

d. Subtract using 2's complement:

i) $(111001)_2 - (101011)_2$ ii) $(11010)_2 - (1010110)$ **(04 Marks)**

8 a. Select the correct answer :

i) The basic gates are

A) NAND and NOR B) NOT, AND and OR

C) EXOR and EXNOR D) None of these.

ii) $A + \overline{A}$ is

A) A B) 0 C) 1 D) None of these.

iii) To add $(1010)_2$ and $(1101)_2$ binary numbers, we need _____ full adders.

A) 1 B) 2 C) 3 D) 4

iv) The output expression for EX-OR is

A) A + B B) $A\overline{B} + \overline{A}B$ C) $\overline{A}\,\overline{B} + AB$ D) None of these. **(04 Marks)**

b. Simplify the following Boolean expressions:

i) $Y = (A + \overline{B} + \overline{C})(A + \overline{B} + C)$

ii) $Y = A[B + C(\overline{AB + AC})]$ **(06 Marks)**

c. Explain the operation of DTL NOR gate. **(06 Marks)**

d. Realize a parallel binary adder for the following binary numbers:

i) $(1011)_2$ ii) $(1101)_2$ **(04 Marks)**

* * * * *